WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming a first substantially H-shaped mask material and a second substantially H-shaped mask material on a main surface of a semiconductor substrate, said first mask material having a first portion, a second portion, and a third portion connected in that order along a first direction in plan view and wherein a dimension of said second portion with respect to a second direction in plan view that is perpendicular to said first direction is smaller than dimensions of said first and third portions with respect to said second direction, said second mask material having a fourth portion, a fifth portion, and a sixth portion connected in that order along said first direction and wherein a dimension of said fifth portion with respect to said second direction is smaller than dimensions of said fourth and sixth portions with respect to said second direction, so that said first and fourth portions, said second and fifth portions, and said third and sixth portions are each mutually spaced apart and aligned along said second direction;

(b) etching said semiconductor substrate using said first and second mask materials as etch masks, to form in said main surface a recessed portion having a first side surface, a second side surface, and a third side surface that are defined by said semiconductor substrate below said first to third portions, and a fourth side surface, a fifth side surface, and a sixth side surface that are defined by said semiconductor substrate below said fourth to sixth portions;

(c) implanting impurity ions in said second direction from diagonally above, with said first and second mask materials being formed on said main surface, to form first doped channel regions of a first conductive type only in said second and fifth side surfaces among said first to sixth side surfaces;

(d) forming an element isolating insulation film by filling said recessed portion to define respective portions of said semiconductor substrate where said first and second mask materials are formed in said step (a) as a first element forming region and a second element forming region, said step (d) being performed after said step (c);

(e) forming second doped channel regions of said first conductive type respectively within said main surface that is in said first and second element forming regions;

(f) removing said first and second mask materials, said step (f) being performed after said step (c);

(g) forming an insulating film on said main surface that is in said first and second element forming regions, said step (g) being performed after said step (f);

(h) forming a conductive film on a structure obtained by said step (g);

(i) patterning said conductive film to form a gate electrode above said main surface on which said second and fifth portions are formed in said step (a), said gate electrode extending along said second direction;

(j) forming first source-drain regions of a second conductive type being different from said first conductive type, in said main surface in which said first and fourth portions are formed in said step (a); and

(k) forming second source-drain regions of said second conductive type in said main surface in which said third and sixth portions are formed in said step (a).

2. The method according to claim 1, wherein the following relationship holds:

$$\tan^{-1}(W2/T) < \alpha \leq \tan^{-1}(W1/T)$$

where W2 is an interval between said first portion and said fourth portion and an interval between said third portion and said sixth portion; W1 is an interval between said second

portion and said fifth portion; α is an angle formed by an implant direction of said impurity in said step (c) and a direction of the normal to said main surface; and T is a film thickness of said first and second mask materials.

3. The method according to claim 1, further comprising the steps of:

(l) forming an interlayer dielectric film, said step (l) being performed after said steps (i) through (k);

(m) forming, in said interlayer dielectric film, contact holes connected to said second source-drain regions;

(n) forming electrically conductive plugs in said contact holes;

(o) forming a capacitor lower electrode connected to said electrically conductive plugs;

(p) forming a capacitor dielectric film on said capacitor lower electrode; and

(q) forming a capacitor upper electrode on said capacitor dielectric film.

4. The method according to claim 3, wherein:

said electrically conductive plugs are made of a semiconductor to which an impurity of said second conductive type is added; and

further comprising the step of (r) introducing an impurity into said main surface through said contact holes to form an impurity-introduced region of said second conductive type, said step (r) being performed between said steps (m) and (n).

5. The method according to claim 3, wherein:

in said step (a), a third mask material is further formed on said main surface, said third mask material opposing and spaced apart from said third portion and aligned

with said first mask material along said first direction;

in said step (b), said semiconductor substrate is etched using said first to third mask materials as an etch mask, whereby said recessed portion is formed; and

further comprising the step of (s) implanting ions of an impurity in said first direction from diagonally above, with said first and third mask materials being formed on said main surface, to form an impurity-implanted region of said second conductive type in said third side surface, said step (s) being performed before said step (d).

6. The method according to claim 5, wherein:

$\tan^{-1}(V/U) \leq \beta \leq \tan^{-1}(V/T)$

is satisfied, where V is an interval between said first mask material and said third mask material; β is an angle formed by an implant direction of said impurity in said step (s) and a direction of the normal to said main surface; T is a film thickness of said third mask material; and U is a depth from an upper surface of said third mask material to a bottom surface of said recessed portion.

7. The method according to claim 3, further comprising the step of (t) introducing an impurity into a bottom surface of said recessed portion through said recessed portion to form a first channel cut region of said first conductive type, said step (t) being performed after said step (b) and before said step (d).

8. The method according to claim 7, wherein:

said semiconductor substrate has a memory cell array section and a peripheral circuit section;

said first channel cut region is formed in said memory cell array section; and

further comprising the step of (u) forming a mask material so as to cover said peripheral circuit section, said step (u) being performed before said step (t).

9. The method according to claim 7, wherein:

said semiconductor substrate has a memory cell array section and a peripheral circuit section;

said first channel cut region is formed in said memory cell array section;

in said step (t), said impurity is introduced also into said peripheral circuit section to form a second channel cut region in said peripheral circuit section; and

further comprising the step of (v) introducing an impurity of said second conductive type into said peripheral circuit section to cancel out said second channel cut region, said step (v) being performed after said step (t).

10. The method according to claim 1, wherein said step (e) is performed after said step (g).

11. A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming a first mask material, a second mask material, and a third mask material on a main surface of a semiconductor substrate, said first mask material having a first portion, a second portion, and a third portion connected in that order along a first direction in plan view, said second mask material having a fourth portion, a fifth portion, and a sixth portion connected in that order along said first direction, and said third mask material having a seventh portion, an eighth portion, and a ninth portion connected in that order along said first direction, so that said third, fourth and ninth portions are mutually spaced apart and aligned in that order along a second direction in plan view that is

perpendicular to said first direction, that said second and eighth portions are mutually spaced apart and aligned along said second direction, and that said second and fifth portions are not aligned along said second direction;

(b) etching said semiconductor substrate using said first to third mask materials as an etch mask to form in said main surface a recessed portion having a first side surface, a second side surface, and a third side surface that are defined by said semiconductor substrate below said first to third portions, respectively, a fourth side surface, a fifth side surface, and a sixth side surface that are defined by said semiconductor substrate below said fourth to sixth portions, respectively, and a seventh side surface, an eighth side surface, and a ninth side surface that are defined by said semiconductor substrate below said seventh to ninth portions;

(c) implanting impurity ions in said second direction from diagonally above, with said first to third mask materials being formed on said main surface, to form first doped channel regions of a first conductive type only in said second side surface of said second and third side surfaces, only in said fifth side surface of said fourth and fifth side surfaces, and only in said eighth side surface of said eighth and ninth side surfaces;

(d) forming an element isolating insulation film by filling said recessed portion to define respective portions of said semiconductor substrate where said first to third mask materials are formed in said step (a) as a first element forming region, a second element forming region, and a third element forming region, said step (d) being performed after said step (c);

(e) forming second doped channel regions of said first conductive type within said main surface that is in said first to third element forming regions, respectively;

(f) removing said first to third mask materials, said step (f) being performed after said step (c);

(g) forming an insulating film on said main surface that is in said first to third element forming regions, said step (g) being performed after said step (f);

(h) forming a conductive film on a structure obtained by said step (g);

(i) patterning said conductive film to form a gate electrode above said main surface on which said second, fifth, and eighth portions are formed in said step (a), said gate electrode extending along said second direction;

(j) forming first source-drain regions of a second conductive type being different from said first conductive type, in said main surface in which said first, sixth, and seventh portions are formed in said step (a); and

(k) forming second source-drain regions of said second conductive type in said main surface in which said third, forth, and ninth portions are formed in said step (a).

12. The method according to claim 11, wherein the following relationship holds:

$\tan^{-1}(W2/T) < \alpha \leq \tan^{-1}(W1/T)$

where W2 is an interval between said third portion and said fourth portion and an interval between said fourth portion and said ninth portion; W1 is an interval between said second portion and said eighth portion; α is an angle formed by an implant direction of said impurity in said step (c) and a direction of the normal to said main surface; and T is a film thickness of said first to third mask materials.

13. The method according to claim 11, further comprising the steps of:

(l) forming an interlayer dielectric film, said step (l) being performed after said steps (i) through (k);

(m) forming, in said interlayer dielectric film, contact holes connected to said second source-drain regions;

(n) forming electrically conductive plugs in said contact holes;

(o) forming a capacitor lower electrode connected to said electrically conductive plugs;

(p) forming a capacitor dielectric film on said capacitor lower electrode; and

(q) forming a capacitor upper electrode on said capacitor dielectric film.

14. The method according to claim 13, wherein:

said electrically conductive plugs are made of a semiconductor to which an impurity of said second conductive type is added; and

further comprising the step of (r) introducing an impurity into said main surface through said contact holes to form an impurity-introduced region of said second conductive type, said step (r) being performed between said steps (m) and (n).

15. The method according to claim 13, wherein:

in said step (a), a fourth mask material is further formed on said main surface, said fourth mask material opposing and spaced apart from said third portion and aligned with said first mask material along said first direction;

in said step (b), said semiconductor substrate is etched using said first to fourth mask materials as an etch mask, whereby said recessed portion is formed; and

further comprising the step of (s) implanting ions of an impurity in said first direction from diagonally above, with said first and fourth mask materials being formed on said main surface, to form an impurity-implanted region of said second conductive type in said third side surface, said step (s) being performed before said step (d).

16. The method according to claim 15, wherein the following relationship holds:

$$\tan^{-1}(V/U) \leq \beta \leq \tan^{-1}(V/T)$$

where V is an interval between said first mask material and said fourth mask material; β is an angle formed by an implant direction of said impurity in said step (s) and a direction of the normal to said main surface; T is a film thickness of said fourth mask material; and U is a depth from an upper surface of said fourth mask material to a bottom surface of said recessed portion.

17. The method according to claim 13, further comprising the step of (t) introducing an impurity into a bottom surface of said recessed portion through said recessed portion to form a first channel cut region of said first conductive type, said step (t) being performed after said step (b) and before said step (d).

18. The method according to claim 17, wherein:

said semiconductor substrate has a memory cell array section and a peripheral circuit section;

said first channel cut region is formed in said memory cell array section; and

further comprising the step of (u) forming a mask material so as to cover said peripheral circuit section, said step (u) being performed before said step (t).

19. The method according to claim 17, wherein:

said semiconductor substrate has a memory cell array section and a peripheral circuit section;

said first channel cut region is formed in said memory cell array section;

in said step (t), said impurity is introduced also into said peripheral circuit section to form a second channel cut region in said peripheral circuit section; and

further comprising the step of (v) introducing an impurity of said second conductive type into said peripheral circuit section to cancel out said second channel cut region, said step (v) being performed after said step (t).

20. A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming an insulating film on a main surface of a semiconductor substrate;

(b) forming a conductive film on said insulating film;

(c) implanting ions of an impurity into said main surface through said conductive film and said insulating film to form doped channel regions;

(d) patterning said conductive film to form a gate electrode; and

(e) introducing an impurity into said main surface that is exposed from said gate electrode to form source-drain regions.